REMARKS

File History

In the first substantive Office action of 2/24/2005, the following rejections, objections and other actions appear to have been made:

> Claims 2, 4-7, 13-17, 19-24 were objected to for depending from a rejected base claim but were otherwise indicated to contain allowable subject matter.

> Claims 1, 3, 8-12, 18, 25- 27 were rejected under 35 USC §102(b) as being fully anticipated by **Turner** (U.S. Pat. 5,339,311).

> Findings of fact were made re the apparent teachings of Turner to one of ordinary skill in the art.

Summary of Current Response

Claims 1-10, 13-25 are amended.

Claim 12 is cancelled.

Claims 28-41 are newly presented.

Arguments are presented concerning the applied art, its proposed combination and its applicability to various ones of the claims. The amendments to claims are not made to overcome the applied art but rather to improve the forms of the claims.

Applicants' Overview of Outstanding Office Action

Applicant sees the outstanding Office action of 12/29/2004 as having the following major features:

(1) Selector circuit 45 of Fig. 4 in Turner '311 was **deemed to be equivalent to** the disclosed test-and-reshuffle circuit (i.e. item 213 of application Fig. 3) of the present application.

(2) The combination of the Turner's re-sequencing buffer 44 (RB, Fig. 2) and re-sequencing buffer controller 46 (RBC, Fig. 2) was **deemed to be equivalent to** the disclosed double-back shifter.

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Applicant's reading of the applied Turner '311 reference

The Examiner is correct in noting that both Turner '311 and the present application are directed to the problem of re-sequencing informational units after they have traversed through paths of possibly different delay within a switch fabric and emerged out of proper order.

Turner's solution to the problem is substantially different from that of the claimed subject matter. Please note that Claim 1 above has been amended to include recitation of: "(b) .... reshuffling at least the relative logical order of the tested units **within** the double-back shifter" (emphasis added).

Turner does not reshuffle the order of stored informational units **within a shifter**. Instead, as better seen in Turner Fig. 2, most of the data stands relatively still within respective slots of one of buffers 44 (RB) and 48 (XMB) while a singular piece of informational data is selectively moved out of the RB buffer 44 and stored into the sequence of data building up within the transmit buffer 48 (XMB).

The one, moved item of Turner '311 arrives in the transmit buffer 48 (XMB) only **after having won a seniority contest** carried out among contestants residing only in the RB buffer 44. Residents of the transmit buffer 48 (XMB) do not participate in the RB seniority contest or any other comparison contest. Thus the transmit buffer 48 (XMB) cannot be reasonably seen as constituting part of a shift mechanism whose contents are tested against one another. In Turner, only contents of the RB buffer 44 are tested against one another, and then, there is no reshuffling of their relative order within the RB buffer 44. Instead, one and only one item leaves the RB buffer 44 after having been declared the winner of the **seniority**

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contest. There is no concurrent reshuffling of logical storage position for plural ones of Turner's payloads.

In terms of more specific details, Turner calls for the generation of a set of constantly-incremented, relative ages for the contestants residing in the RB buffer 44. Age is defined by Turner as the difference between current time (always advancing) and initial send time (the time that the packet was initially input into the switch fabric), where such a send time is stamped on by the Time Stamp controller 38 of Turner Fig. 2.

In order to determine who is the most senior of the aging packets residing in the RB buffer 44 (Fig. 2), Turner performs a marching ones ("1") elimination contest along a wired-OR circuit. Details of that marching ones ("1") contest are provided in the discussion of Turner Fig. 5. Briefly, the most significant age bit for each buffer slot (RB slot) aligns on the right side of each shift register (each BSR 60). All participating contestants simultaneously march their MSB out onto the wired OR line. Each contestant that succeeds in showing a logic 1 for that first bit-by-bit shift, is a winner, provided there is at least one other contestant who shows a "1". Any contestant that cannot match the high 1's of the winners is a "loser" (col. 5, line 7) and drops out of the contest. A corresponding elimination flip flop is flipped to indicate the slot has lost and is no longer in play for the next step in the bit-by-bit elimination contest. Then all remaining contestants show their next highest bit, losers drop out, and so on. At the end of the seniority show-off parade there will usually be one, most-aged packet remaining. However, ties are possible (col. 2, lines 41-43), in which case, the slot numbers are used to break ties and pick the one contestant who wins a glamorous vacation trip to the transmit buffer 48 (to the XMB of Fig. 2 --a bit of humor obviously being injected here).

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The point made here is that, ... yes, Turner '311 does disclose shift registers (BSR's 60). However, their function is nothing akin to that of the double-back shifter recited in the

originally filed claims. The function of Turner's BSR's (bi-directional shift registers 60) is to implement the bit-by-bit seniority elimination contest. See col. 4, line 49 for example.

Stated otherwise, Turner's shift registers 60 are not used for shifting sequence values in opposed directions across opposed input ports of test-and-reshuffle circuits. There are no re-shuffle circuits in Turner for re-shuffling the order of information units while they are held in a shifter. (Note: Due to an obvious numbering error, Turner '311 has two different items both referenced as "60". Buffers 58, 60 of Fig. 2 are used for internal device testing. BSR's 60 of Figs. 3 & 5 march the most significant bits out onto the contention bus (the wired OR) during the seniority establishing elimination rounds.)

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Claim 1 compared against Turner '311

Claim 1 is amended above to clarify that the "(b) ... first test-and-reshuffle circuit [is] for reshuffling at least the relative logical order of the tested units within the double-back shifter if said testing shows the tested information units to be out of proper relative sequential order ... " (underlining and bracket text added).

Turner does not have a shifter within whose storage areas, contents are tested against one another, and then reshuffled within the same shifter if the test shows that the tested items are out of relative order with respect to one another. Turner '311 does not suggest a reshuffling of contents within a shifter. Instead, Turner teaches away from such an idea by guiding the ordinary artisan to move only the most senior packet (the winner) out from its slot in the elimination contest area (the RB 44) and into the next sequential slot in the transmit buffer (the XMB 48). Data is not reshuffled from one slot to another slot within Turner's RB buffer 44. Data is not cross-tested, one against the other in Turner's XMB buffer 48.

In view of the above, Claim 1 is clearly distinguishable over the teachings of Turner '311. Claims 2, 4-7, 13-17 depend from Claim 1 and have already been indicated to contain allowable subject matter. Nonetheless, some of these claims are amended herein so that their language comports with that of amended base Claim 1.

With respect to Claim 3, Turner does not teach or suggest a circuit that "selectively reorders ... information units stored in ... [a] double-back shifter according to said comparisons" (underlining and bracketed text added). As explained above, the transmit buffer (XMB 48) of Turner Fig. 2 cannot be deemed to be part of a shifter whose residents are tested against one another because the residents of Turner's XMB 48 are not tested against one

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another. Each has already won, earlier on, in the elimination contest carried on within the RB buffer 44. That RB buffer is not a shifter.

With respect to Claim 9, Turner does not mention anything about a distributed multi-shelf system.

With respect to Claim 10, Turner does not mention anything about cross-testing packets from different sources. The slot numbers of Turner '311 identify the slots within RB 44 where the contestants happen to reside during the seniority contest. These residence addresses have nothing to do with the location from where the contestants originally came prior to arriving in the slots of the RB buffer. The RB slot numbers are used merely as arbitrary tie breakers. It is as if the judge in a senior citizen beauty contest finds to his dismay that the last two remaining contestants have exactly the same age. The judge then decides to break the tie and award the prize to the one contestant whose house number happens to be the largest. This arbitrary tie-breaking mechanism has nothing to do with where the contestants originally came from.

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Claim 18 compared against Turner '311

With respect to method Claim 18, the distinction over Turner is even stronger. Claim 18 has been amended to clarify that step (b) of repetitively comparing, reordering and shifting occurs for "the sequence indicated information units within the double-back shifter" and that the result is "so as to cause the information units to be in proper indicated sequence when shifted out of said double-back shifter" (emphasis added).

Turner does not repetitively compare, reorder and shift data within his receive buffer (RB 44). The act of removing the most senior (most aged) packet out of the non-shifting RB 44 and into the XMB 48 does not constitute a reordering of data within a double-back shifter. There is no "order" to the one data item moved out of Turner's receive buffer (RB 44) because that data is moved out alone. A single data item cannot be reasonably said to be within an order. Of course, data items are in aged order within Turner's transmit buffer (XMB 48). However, at that stage, there is no comparing of the stored data and no reordering of the stored data. Accordingly, neither of Turner's RB buffer 44 and XMB buffer 48 can be deemed to perform steps equivalent to those recited in Claim 18.

With respect to Claim 25, Turner does not teach or suggest a multi-row shifter.

With respect to Claim 26, Turner does not teach or suggest "information units having source indicators indicating a same source". The slot numbers of Turner's RB 44 have not been shown to have any relationship to where the routed data came from.

With respect to Claim 27, Turner does not teach or suggest "information units having valid entry indicators indicating valid entries". The slot numbers of Turner's RB 44 have not been shown to have any relationship to whether they contain valid data or not.

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CONCLUSION

In light of the foregoing, Applicant respectfully requests further reconsideration and withdrawal of the outstanding grounds of rejection. Should any other action be contemplated by the Examiner, it is respectfully requested that he contact the undersigned at (408) 392-9250 to discuss the application.

The Commissioner is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 50-2257 for any matter in connection with this response, including any fee for extension of time (requested here) and/or fee for additional claims, which may be required for continued pendency of the application.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on June 24, 2005.

[signature] 6-24-05

Attorney for Applicant(s) Date of Signature

Respectfully submitted,

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